

Atty. Dkt. No. 077311-0120
Serial No.; 10/010,547

Amendments to the Claims:

Please amend the claims as follows:

Please cancel Claims 4 and 14 without prejudice or disclaimer.

1. (Currently Amended) A high-speed digital multiplexer including:

a plurality of input pins for receiving a plurality of digital input signals;

switching circuitry coupled to the input pins, the switching circuitry

having respective outputs coupled to a common node, the switching circuitry operative to enable a selected one of the plurality of input pins;

a ~~local-signal-converter~~ transresistance amplifier having a circuit branch set to a common voltage, the branch connected to the common node to sense changes in current corresponding to an input signal received by an enabled input pin; and

an output pin coupled to the ~~local-signal-converter~~ transresistance amplifier, whereby the ~~local-signal-converter~~ transresistance amplifier is operative to produce voltage changes at the output corresponding to the sensed current changes.

2. (Original) A high-speed digital multiplexer according to claim 1 wherein the switching circuitry comprises:

a plurality of semiconductor switches, the plurality of semiconductor switches corresponding to the plurality of input pins.

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3. (Original) A high-speed digital multiplexer according to claim 2 wherein the plurality of semiconductor switches comprises a plurality of diodes,

4. (Cancelled)

5. (Currently Amended) A high-speed digital multiplexer according to claim [[4]] 1 wherein the transresistance amplifier includes:

- a base terminal fixed to a constant voltage;
- an emitter branch coupled to the common node; and
- a collector terminal tied to the output pin.

6. (Currently Amended) A high-speed digital multiplexer for use with a device-interface-board, the device-interface-board adapted for coupling to automatic test equipment, the multiplexer including:

- a plurality of input pins adapted for coupling to a plurality of automatic test equipment channels;
- switching circuitry coupled to the input pins, the switching circuitry having respective outputs coupled to a common node, the switching circuitry operative to enable a selected one of the plurality of input pins;

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a local signal converter having a circuit branch set to a common voltage,
the branch connected to the common node to sense changes in current corresponding to input
signal received by an enabled input pin; and

an output pin coupled to the local signal converter, whereby the local
signal converter is operative to produce voltage changes at the output corresponding to the sensed
current changes; and

wherein the switching circuitry is operative to enable the selected one of
the plurality of input pins based on the selected one of the plurality of input pins having a lower
first voltage than non-selected ones of the plurality of input pins.

7. (Original) A high-speed digital multiplexer according to claim 6 wherein the
switching circuitry comprises:

a plurality of semiconductor switches, the plurality of semiconductor
switches corresponding to the plurality of input pins.

8. (Original) A high-speed digital multiplexer according to claim 7 wherein the
plurality of semiconductor switches comprises a plurality of diodes.

9. (Original) A high-speed digital multiplexer according to claim 6 wherein the
local signal converter comprises:

a transresistance amplifier.

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10. (Original) A high-speed digital multiplexer according to claim 9 wherein the transresistance amplifier includes:

- a base terminal fixed to a constant voltage;
- an emitter branch coupled to the common node; and
- a collector terminal tied to the output pin.

11. (Currently Amended) A device-interface-board for calibration/validation of automatic test equipment, the device-interface-board including:

- at least one test socket adapted for receiving a device-under-test; and
- a high-speed digital multiplexer for selectively passing tester signals from the automatic test equipment to the test socket, the multiplexer including
 - a plurality of input pins adapted for coupling to a plurality of automatic test equipment channels,
 - switching circuitry coupled to the input pins, the switching circuitry having respective outputs coupled to a common node, the switching circuitry operative to enable a selected one of the plurality of input pins,
 - a ~~local signal converter~~ transresistance amplifier having a circuit branch set to a common voltage, the branch connected to the common node to sense changes in current corresponding to an input signal received by an enabled input pin, and

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an output pin coupled to the ~~local signal converter~~ transresistance amplifier, whereby ~~local signal converter~~ transresistance amplifier is operative to produce voltage changes at the output corresponding to the sensed current changes.

12. (Currently Amended) A ~~device-interface-board high-speed-digital-multiplexer~~ according to claim 11 wherein the switching circuitry comprises:

a plurality of semiconductor switches, the plurality of semiconductor switches corresponding to the plurality of input pins.

13. (Currently Amended) A ~~device-interface-board high-speed-digital-multiplexer~~ according to claim 12 wherein the plurality of semiconductor switches comprises a plurality of diodes.

14. (Cancelled)

15. (Currently Amended) A ~~device-interface-board high-speed-digital-multiplexer~~ according to claim ~~14~~ 11 wherein the transresistance amplifier includes:

a base terminal fixed to a constant voltage;

an emitter branch coupled to the common node; and

a collector terminal tied to the output pin.

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16. (Withdrawn - Currently Amended) A method of selecting one from a plurality of high-speed digital input signals applied to a plurality of input pins, the input pins coupled through switching circuitry to a common node, the method comprising the steps:

applying a constant voltage to the common node;

activating the pin corresponding to the selected input signal;

maintaining a reverse-bias condition at diodes corresponding to non-selected input signals;

detecting current changes at the common node caused by the selected input signal; and

producing output voltage changes corresponding to the detected current changes.

17. (New) A high-speed digital multiplexer according to claim 1 wherein the switching circuitry is operative to enable the selected one of the plurality of input pins based on the selected one of the plurality of input pins having a lower first voltage than non-selected ones of the plurality of input pins.

18. (New) A high-speed digital multiplexer according to claim 17 wherein the common voltage is higher than the first voltage and at least one voltage of the non-selected ones of the plurality of input pins is higher than the common voltage.

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19. (New) A high-speed digital multiplexer according to claim 6 wherein the common voltage is higher than the first voltage and at least one voltage of the non-selected ones of the plurality of input pins is higher than the common voltage.

20. (New) A device-interface-board according to claim 11 wherein the switching circuitry is operative to enable the selected one of the plurality of input pins based on the selected one of the plurality of input pins having a lower first voltage than non-selected ones of the plurality of input pins.

21. (New) A device-interface-board according to claim 20 wherein the common voltage is higher than the first voltage and at least one voltage of the non-selected ones of the plurality of input pins is higher than the common voltage.

22. (New) A method according to claim 16, wherein the step of activating comprises:

driving a non-selected signal to a voltage higher than the common voltage; and

driving the selected input signal to a voltage lower than the common voltage.

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